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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,200	06/27/2003	Shion-Hau Liaw	3313-1009P	5799

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EXAMINER	
YOHA, CONNIE C	
ART UNIT	**PAPER NUMBER**
2827	

DATE MAILED: 07/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:D

Office Action Summary	Application No.	Applicant(s)	
	10/607,200	LIAW ET AL.	
	Examiner	Art Unit	
	Connie C. Yoha	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters; prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4 and 12-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,8-10,13 and 16* is/are rejected.

7)☒ Claim(s) *4, 6-7, 12, 14-15, 17-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/27/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Connie C. Yoha

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The Amendment filed on 6/22/05 has been entered and are made of record.

2. Claims 1, 4-9, 12-16 are amended.

3. Claim 3 and 11 are canceled.

4. Claim 17 and 18 are newly added.

5. Claims 1-2, 4-10, 12-18 are pending.

Response to Arguments

6 Applicant's argument filed 6/22/05 has been fully considered.

Applicant's arguments with respect to claims 1-2, 4-10, 12-18 has been considered but are moot in view of the new ground(s) of rejection due to the amended claims.

Previously cited reference Nojima (6222765) and Ratnakumar et al (6556487) are again used to rejected the amended claims. Examiner especially like to point out that in Nojima's reference do teaches the SRAM unit (fig. 2, 110) and a non-volatile unit (fig. 2, either 150 and 152 or 154 and 156 can be used as the non-volatile unit) (col. 3, line32-35), where the non-volatile unit comprises two split-gate transistor (fig. 2, either 150 and 152 or 154 and 156) where the gate of the two split-gate transistor are connected using to either WL1 or WL2 depending on which pair of the two transistors are used as the non-volatile unit and the source of the two split-gate transistor are connected to a common voltage level (fig. 2, to the source line S). The detail claims rejection can be found below.

Claim Rejections - 35 USC ∋ 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1, 5, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Nojima, Pat. No. 6222765 (previous cited).

With regard to claim 1, Nojima discloses a non-volatile static random access memory (SRAM) cell, comprising: an SRAM unit (fig. 2, 110), which receives a 1-bit datum, temporarily stores the 1-bit datum, and transmits the 1-bit datum for normal operation; and a non-volatile memory unit (fig. 2, 150, 152, 154, and 156), which connects to the SRAM unit for storing the 1-but datum in the SRAM unit before power is turned off (storage operation), keeping the 1-bit datum (storage operation), recovering the 1-bit datum back to the SRAM unit once the power supply is resumed (recovery operation), and erasing the 1-bit after the recovery operation is completed (erase operation) (col. 4, line 26-67), the non-volatile memory unit further including two split-gate transistors (fig. 2, 150 and 152 or 154 and 156) (col. 3, line 32-40), each of the split-gate transistors including a control gate, a source and a drain, the control gates of the split-gate transistors being connected (fig. 2, where the two transistor 150 and 152 are connected to the same WL1 or the transistor 154 and 156 are connected to the

same WL2), the sources of the split-gate transistors being connected and having a same voltage level (fig. 2, source of 150 and 152 are connected and having a same voltage level S) (col. 3, line 50-53), the drains of the split-gate transistors storing the 1-bit datum in the SRAM unit (fig. 2, the drain of 150 and 152 or 154 and 156 are connected to the BL and /BL of which is connected to the storage node of the SRAM 130 and 132).

With regard to claim 5 and 8, Nojima discloses wherein a voltage on the control gates of the split-gate transistors is 0V and a voltage on the source of the split-gate transistors is 0V during the normal operation (col. 3, line 63-65).

Claim Rejections - 35 USC э 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2, 9-10, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nojima, Pat. No. 6222765 (previously cited) in view of Ratnakumar et al, Pat. No. 6556487 (previously cited).

With regard to claim 2, Nojima, as applied in prior rejection, disclosed all claimed subject matter including wherein the SRAM unit further comprises a pair of inverters (fig. 2, 112 and 116 and 114 and 118). Nojima does not disclose the SRAM unit further comprises two n-channel metal oxide semiconductor field effect transistors (nMOSFET's), the gates of the nMOSFET's connecting to a word line. However, Ratnakumar disclose a non-volatile static memory cell device using one type of SRAM, having two n-channel metal oxide semiconductor field effect transistors (nMOSFET's) with their gates connecting to a word line (fig. 8, T1 and T2 connecting to VWL) as an access transistor to access the SRAM unit. Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to replace the use of the type of SRAM unit of Ratnakumar's in place of Nojima's that have two n-MOSFET's activated by the word line voltage to operate as the access transistors to access the SRAM unit when in use.

With regard to claim 9, Nojima discloses a non-volatile static random access memory (SRAM) cell, comprising: an SRAM unit (fig. 2, 110), which comprises a first transistor (fig. 2, 112), a second transistor (fig. 2, 114), a third transistor (fig. 2, 116), a fourth transistor (fig. 2, 118), a fifth transistor (fig. 2, 120), and a sixth transistor (fig. 2, 112), wherein the first transistor (fig. 2, 112) and the third transistor (fig. 2, 116) form a first inverter, the second (fig. 2, 114) and the fourth (fig. 2, 118) forms a second inverter, the gates of the first transistor and the third transistor are connected to the drains of the fourth transistor and the sixth transistor (fig.2), the gates of the second transistor and the fourth transistor are connected to the drains of the first transistor, the third transistor,

and the fifth transistor; and a non-voltage memory unit (fig. 2, 150, 152, 154, 156), which connects to the SRAM unit (fig. 2, 110) and comprise a seventh transistor (fig. 2, 150 or 154) and an eight transistor (fig. 2, 152 or 156), the seventh transistor (fig. 2, 150 or 154) and the eighth transistor (fig. 2, 152 or 156) being split-gate transistors, each of the split-gate transistors including a control gate, a source and a drain, the source of the seventh and eight transistors being connected and having a same voltage level (fig. 2, voltage level S) (col. 3, line 50-53), the control gates of the seventh transistor (fig. 2, control gate of 150 or 154) and the eight transistor (fig. 2, control gate of 152 or 156) being connected (fig. 2, being connected to the same WL1 or WL2), the drain of the seventh transistor (fig. 2, 150 or 154) and the drains of the first transistor (fig. 2, 112), the third transistor (fig. 2, 116) and the fifth transistor (fig. 2, 120) are connected, and the eighth transistor (fig. 2, 152 or 156) is connected to the drains of the second transistor (fig. 2, 114), the fourth transistor (fig. 2, 118) and the sixth transistor (fig. 2, 122); wherein the SRAM unit (fig. 2, 110) receives a 1-bit datum, temporarily stores the 1-bit datum, and transmits the 1-bit datum for normal operations (col. 3, line 63-col. 4, line 9); and the drains of the seventh and eighth transistors of the non-volatile memory unit stores the 1-bit datum in the SRAM unit before power is turned off (storage operation, keeps the 1-bit datum (storage operation), recovers the 1-bit datum back to the SRAM unit once the power supply is resumed (recovery operation), and erases the 1-bit after the recovery operation is completed (erase operation) (col. 3, line 63-col. 5, line 12).

However, Nojima does not discloses the gates of the fifth transistor and the sixth transistor are connected with a word line. However, Ratnakumar disclose a non-volatile static memory cell device using one type of SRAM, having two n-channel metal oxide semiconductor field effect transistors (nMOSFET's) (equivalent to the fifth and sixth transistors) with their gates connecting to a word line (fig. 8, T1 and T2 connecting to VWL) as being an access transistors to access the SRAM unit. Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to replace the use of the type of SRAM unit of Ratnakumar's in place of Nojima's that have two n-MOSFET's activated by the word line voltage to operate as the access transistors to access the SRAM unit when in use.

With regard to claim 10, Nojima does not discloses Nojima discloses wherein the first transistor, the second transistor, the fifth transistor, and the sixth transistor are nMOSFET's. the third transistor and the fourth transistor are pMOSFET's. However, Nojima discloses the first transistor (fig. 2, 112), the second transistor (fig. 2, 114), the fifth transistor (fig. 2, 120), and the sixth transistor (fig. 2, 122) are pMOSFET's instead of nMOSFET's and the third transistor (fig. 2, 116) and the fourth transistor (fig. 2, 118) are nMOSFET's instead of pMOSFET's as a type of transistors used to make up the SRAM device. It would have been obvious for one having ordinary skill in the art at the time the invention was made to recognized that Nojima's n type MOSFET can be used in place of the p type of MOSFET or vise versa, since it is well known in the semiconductor art that the n and p type of MOSFET's transistors can be used interchangeably.

With regard to claim 13 and 16, Nojima discloses wherein a voltage on the control gates of the split-gate transistors is 0V and a voltage on the source of the split-gate transistors is 0V during the normal operation (col. 3, line 63-65).

Allowable Subject Matter

9. Claim 4, 6-7, 12, 14-15, 17, and 18 are objected as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not show the limitation of wherein a voltage on the control gates of the split-gate transistors is lower than 0V and a voltage on the sources of the split-gate transistors is higher than 5V during the erase operation.

Prior art also does not disclose wherein a voltage on the control gates of the split-gate transistors is higher than that a voltage on the sources of the split-gate transistors during the storage operation.

The prior art of record does not show the limitation of wherein a voltage on the control gates of the split-gate transistors is equal to a voltage on the sources of the split-gate transistors during the erase operation.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP ə 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached at (571) 272-1787. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov should you

have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C.Yoha

July 2005

CONNIE C. YOHA
PRIMARY EXAMINER